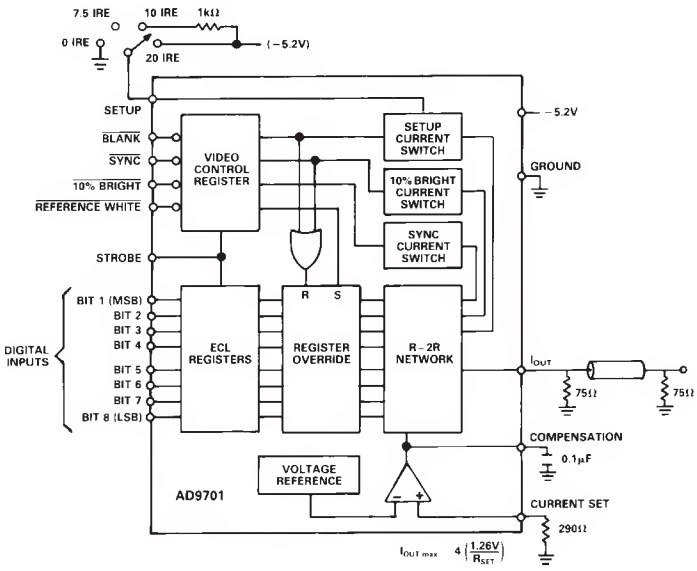
250 MSPS Video Digital-to-Analog Converter

AD9701

FEATURES
250 MSPS Update Rate
Low Glitch Impulse
Complete Composite Functions
Internal Voltage Reference
Single –5.2 V Supply

APPLICATIONS
Raster Scan Displays
Color Graphics
Automated Test Equipment
TV Video Reconstruction

FUNCTIONAL BLOCK DIAGRAM



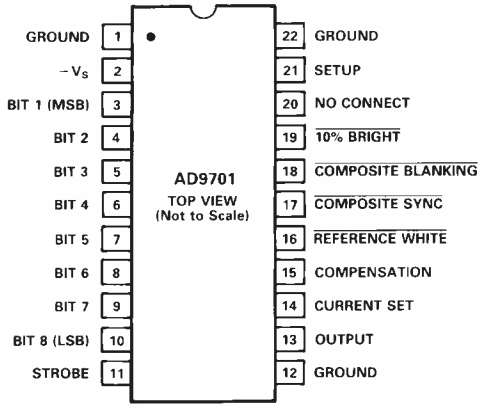
GENERAL DESCRIPTION

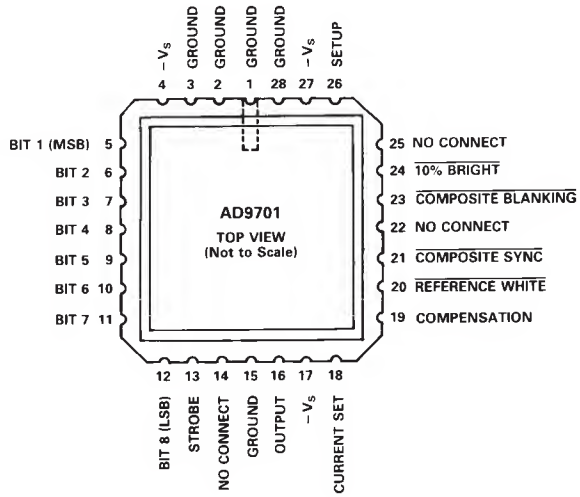
The AD9701 is a high speed, 8-bit digital-to-analog converter with fully integrated composite video functions. High speed ECL input registers provide synchronous operation of data and control functions up to 250 MSPS.

The AD9701 incorporates onboard control functions including horizontal sync, blanking, reference white level and a 10% bright signal for highlighting. The setup level is also adjustable from 0 IRE units to 20 IRE units through the control pin. An internal voltage reference allows the AD9701 to operate as a stand-alone video reconstruction DAC.

The AD9701 is available as an industrial temperature range device, –25°C to +85°C, and as an extended temperature range device, –55°C to +125°C. Both grades of the AD9701 are packaged in a 22-pin ceramic DIP with the extended temperature device also available in a 28-pin LCC package.

PIN CONFIGURATIONS





REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 **World Wide Web Site: http://www.analog.com**
Fax: 617/326-8703

AD9701–SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ($-V_S$) . . . . . –7 V
Digital Input Voltages (Including STROBE, SYNC, BLANKING, 10% BRIGHT and REFERENCE WHITE) . . . . . 0 V to $-V_S$
Analog Output Current . . . . . 37 mA
Power Dissipation (+25°C Free Air)[2] . . . . . 780 mW
Operating Temperature Range
AD9701BQ . . . . . –25°C to +85°C
AD9701SQ/SE . . . . . –55°C to +125°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . +175°C
Lead Soldering Temperature (10 sec) . . . . . +300°C

ELECTRICAL CHARACTERISTICS (Supply Voltages = –5.2 V; R_L = 37.5 Ω; Setup = 0 V, unless otherwise noted)

Parameter	Temp	AD9701BQ Min	AD9701BQ Typ	AD9701BQ Max	AD9701SQ/SE Min	AD9701SQ/SE Typ	AD9701SQ/SE Max	Units
RESOLUTION		8			8			Bits
DC ACCURACY								
Differential Linearity	+25°C		0.25	0.5		0.25	0.5	LSB
	Full			1.0			1.0	LSB
Integral Linearity	+25°C		0.25	0.5		0.25	0.5	LSB
	Full			1.0			1.0	LSB
Monotonicity	Full		Guaranteed			Guaranteed		
INITIAL OFFSET ERROR[3]								
Zero-Scale Offset Error[4]	+25°C		0.05	0.9		0.05	0.9	mV
	Full			0.9			0.9	mV
Zero-Scale Offset Drift Coefficient	Full		2			2		µV/°C
Full-Scale Drift Coefficient	Full		50			50		µV/°C
ANALOG OUTPUT								
Voltage Output[5]								
10% Bright[6]	Full	–0.9	0		–0.9	0		mV
Reference White	Full	–67.45	–71	–74.55	–67.45	–71	–74.55	mV
Blanking (Setup = 0 IRE)[7]	Full	–698.55	–708.5	–718.45	–698.55	–708.5	–718.45	mV
Sync (Setup = 0 IRE)[8]	Full	–979.25	–993.5	–1007.75	–979.25	–993.5	–1007.75	mV
Current Output[5]								
10% Bright[6]	Full	–0.024	0		–0.024	0		mA
Reference White	Full	–1.805	–1.9	–1.996	–1.805	–1.9	–1.995	mA
Blanking (Setup = 0 IRE)[7]	Full	–18.63	–18.9	–19.16	–18.63	–18.9	–19.16	mA
Sync (Setup = 0 IRE)[8]	Full	–26.11	–26.5	–26.87	–26.11	–26.5	–26.87	mA
Output Compliance Range	Full		–1.6; +0.1			–1.6; +0.1		V
Output Resistance	+25°C	640	800		640	800		Ω
DYNAMIC PERFORMANCE								
Update Rate	+25°C	225	250		225	250		MSPS
Output Propagation Delay[9]	+25°C		5	6		5	6	ns
Output Settling Time[10]								
Current	+25°C		8			8		ns
Voltage	+25°C		12			12		ns
Output Slew Rate[11]	+25°C	255	300		255	300		V/µs
Output Rise Time[11]	+25°C		1.7	2.0		1.7	2.0	ns
Output Fall Time[11]	+25°C		1.7	2.0		1.7	2.0	ns
Glitch Impulse	+25°C		60	70		60	70	pV-s
SETUP CONTROL[12]								
Setup Level (Grounded)	Full		0			0		IRE
Setup Level (Open)	Full		7.5			7.5		IRE
Setup Level (Tied to –5.2 V with 1 kΩ)	Full		10			10		IRE
Setup Level (–5.2 V)	Full		20			20		IRE
DIGITAL INPUTS								
Logic "1" Voltage	Full	–1.1			–1.1			V
Logic "0" Voltage	Full			–1.5			–1.5	V
Logic "1" Current	Full			100			100	µA
Logic "0" Current	Full			15			15	µA
Input Capacitance	+25°C		4	5.5		4	5.5	pF
Data Setup Time	+25°C	0.1			0.1			ns
Data Hold Time	+25°C	1.4			1.4			ns

Parameter	Temp	AD9701BQ Min	AD9701BQ Typ	AD9701BQ Max	AD9701SQ/SE Min	AD9701SQ/SE Typ	AD9701SQ/SE Max	Units
POWER SUPPLY[13]								
Supply Current (–5.2 V)	+25°C		140	160		140	160	mA
	Full			160			160	mA
Nominal Power Dissipation	+25°C		728			728		mW
Power Supply Rejection Ratio[14]	Full		3	6		3	6	mV/V

NOTES
[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Typical thermal impedance . . .
22-Pin Ceramic $\theta_{JA} = 64°C/W$; $\theta_{JC} = 16°C/W$
28-Pin Ceramic LCC $\theta_{JA} = 70°C/W$ $\theta_{JC} = 21°C/W$
[3]SYNC, BLANKING, and REFERENCE WHITE are inactive (Logic "1"). $I_{SET} \approx 1.26\ V/R_{SET}$.
[4]All bits at logic HIGH.
[5]All values are relative to full-scale output after being normalized to nominal value. Typical variation in full-scale output from device to device can reach ±10%, for a fixed R_{SET} resistor.
[6]The effect of 10% BRIGHT algebraically adds to the output waveform.
[7]The output level with BLANKING active (Logic "0") is determined by the setup control level.
[8]In normal operation, the BLANKING input is activated (Logic "0") prior to or in conjunction with the SYNC input. The effect of the SYNC output is relative to the setup level.
[9]Measured from edge of STROBE to 50% transition point of the output signal.
[10]Measured with full-scale change in output level, from the 10% transition level to within ±0.2% of the final output value.
[11]Measured from 10% to 90% transition point for full-scale step output.
[12]An IRE unit is 1% of the Grey Scale (GS range) with a 0 IRE setup level.
[13]Supply Voltage should remain stable within ±5% for normal operation.
[14]Measured at ±5% of $-V_S$.

Specifications subject to change without notice.

DIGITAL INPUTS VS. ANALOG OUTPUT

Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	10% Bright	Ref. White	Blanking	Comp. Sync	Analog Output (mV)
1	1	1	1	1	1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1	–71
1	0	0	0	0	0	0	0	0	1	1	1	–320
0	0	0	0	0	0	0	0	0	1	1	1	–637.5
0	0	0	0	0	0	0	0	1	1	1	1	–708.5
X	X	X	X	X	X	X	X	0	0	1	1	0
X	X	X	X	X	X	X	X	1	0	1	1	–71
X	X	X	X	X	X	X	X	0	1	0	1	–637.50[1]
X	X	X	X	X	X	X	X	0	1	0	1	–690.75[2]
X	X	X	X	X	X	X	X	0	1	0	1	–708.50[3]
X	X	X	X	X	X	X	X	0	1	0	1	–779.50[4]
X	X	X	X	X	X	X	X	0	1	0	0	–922.50[1]
X	X	X	X	X	X	X	X	0	1	0	0	–975.75[2]
X	X	X	X	X	X	X	X	0	1	0	0	–993.50[3]
X	X	X	X	X	X	X	X	0	1	0	0	–1064.50[4]
X	X	X	X	X	X	X	X	1	1	0	0	–993.50[1]
X	X	X	X	X	X	X	X	1	1	0	0	–1046.75[2]
X	X	X	X	X	X	X	X	1	1	0	0	–1064.50[3]
X	X	X	X	X	X	X	X	1	1	0	0	–1135.50[4]

NOTES
[1]Setup (Pin 21) grounded (0 IRE units).
[2]Setup (Pin 21) open (7.5 IRE units).
[3]Setup (Pin 21) to –5.2 V through 1 k (0 IRE units).
[4]Setup (Pin 21) to –5.2 V (20 IRE units).

ORDERING GUIDE

Device	Temperature Range	Description	Package Option*
AD9701BQ	–25°C to +85°C	22-Pin DIP, Industrial Temperature	Q-22
AD9701SE	–55°C to +125°C	28-Pin LCC, Extended Temperature	E-28A
AD9701SQ	–55°C to +125°C	22-Pin DIP, Extended Temperature	Q-22

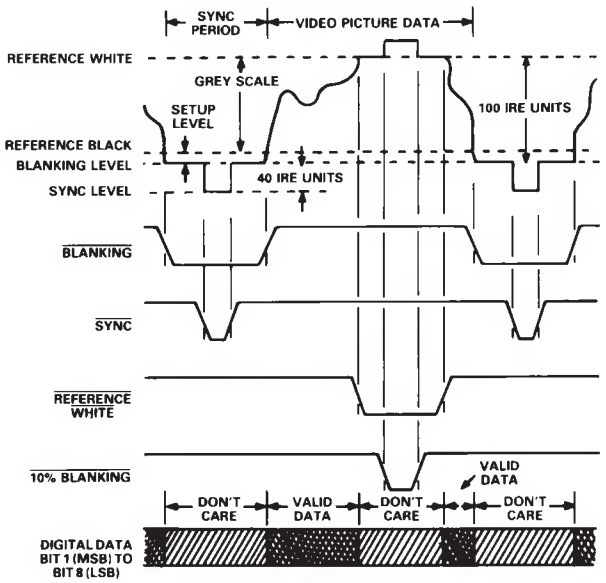
*E = Leadless Ceramic Chip Carrier; Q = Cerdip.

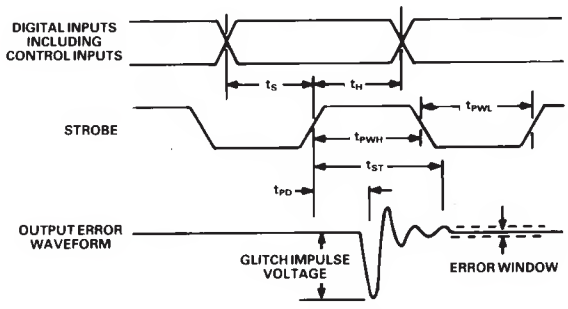
FUNCTIONAL DESCRIPTION

Pin Name	Description
GROUND	One of three ground returns. All grounds should be connected together near the AD9701.
$-V_S$	Negative supply pin, nominally –5.2 V.
BIT 1 (MSB)	One of eight digital input bits. BIT 1 (MSB) is the most-significant-bit of the digital input word.
BIT 2–BIT 7	One of eight digital input bits.
BIT 8 (LSB)	One of eight digital input bits. BIT 8 (LSB) is the least-significant-bit of the digital input word.
STROBE	Data and control register strobe input. STROBE is leading edge triggered.
GROUND	One of three ground returns. All grounds should be connected together near the AD9701.
SETUP	The SETUP input determines the position of the blanking level relative to the "reference black" level (all data bits at logic "0"). The setup level is adjustable from 0 IRE units to 20 IRE units below the reference black level (an IRE unit is 1% of the "grey scale" range).
$\overline{\text{10\% BRIGHT}}$	$\overline{\text{10\% BRIGHT}}$ adds an additional current to the output level, equal to roughly 10% of the "grey scale" range. The $\overline{\text{10\% BRIGHT}}$ is active logic LOW and operates independently of all other inputs.
$\overline{\text{COMPOSITE BLANKING}}$	The $\overline{\text{COMPOSITE BLANKING}}$ input, active logic LOW, forces output to the blanking level set with the SETUP input.
$\overline{\text{COMPOSITE SYNC}}$	The $\overline{\text{COMPOSITE SYNC}}$ input, active LOW, creates a negative going horizontal synchronization pulse relative to the blanking level. Under normal operating conditions, the $\overline{\text{COMPOSITE BLANKING}}$ signal should precede and extend past the $\overline{\text{COMPOSITE SYNC}}$ signal. See SETUP for additional information.
$\overline{\text{REFERENCE WHITE}}$	The $\overline{\text{REFERENCE WHITE}}$ input, active LOW, overrides the data inputs and forces the output to the maximum "grey scale" level.
COMPENSATION	The COMPENSATION input insures adequate gain stability for the internal reference amplifier. Under normal operating conditions, the COMPENSATION input is decoupled to ground through a 0.1 μF capacitor.
CURRENT SET	The CURRENT SET input determines the full-scale or "grey scale" range. The effects of the video control functions are in addition to the "grey scale" range. ($168\ \Omega \le R_{SET} \le 600\ \Omega$). $I_{OUT\,max} \approx 4\ I_{SET} = 4(1.26\ V/R_{SET})$
OUTPUT	Analog output.
GROUND	One of three ground returns. All grounds should be connected together near the AD9701.

SETUP LEVEL	CONFIGURATION (PIN 21)
0 IRE Units	Ground
7.5 IRE Units	Open
10 IRE Units	Connection to –5.2 V through 1 kΩ
20 IRE Units	Connection to –5.2 V

SYSTEM TIMING DIAGRAMS

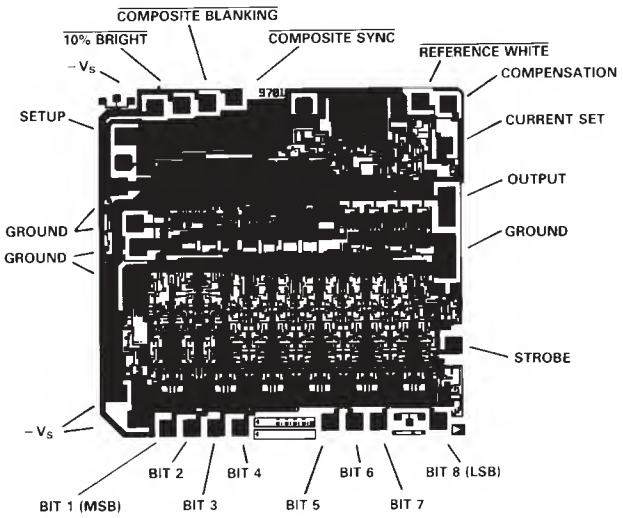




t_S DIGITAL DATA SETUP TIME
t_H DIGITAL DATA HOLD TIME
t_{PWH} STROBE PULSE WIDTH HIGH
t_{PWL} STROBE PULSE WIDTH LOW
t_{ST} SETTLING TIME
t_{PD} MINIMUM PROPAGATION DELAY

NOTES
1. ALL INPUTS, INCLUDING THE VIDEO CONTROL FUNCTIONS, ARE SYNCHRONIZED TO THE STROBE INPUT.
2. THE 10% BRIGHT CONTROL WILL INCREASE THE OUTPUT LEVEL BY APPROXIMATELY 10 IRE UNITS OVER THE PRESENT OUTPUT LEVEL.
3. AN IRE UNIT IS IDEALLY 7.14mV.

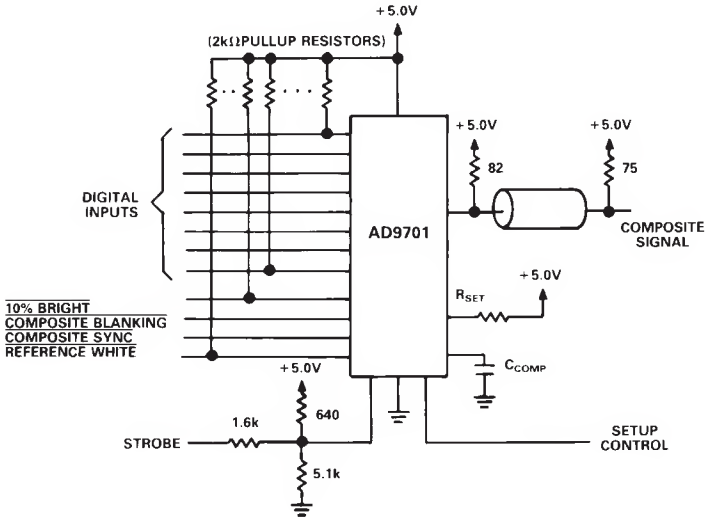
DIE LAYOUT AND MECHANICAL INFORMATION



Die Dimensions . . . . . 107 × 104 × 15 (±2) mils
Pad Dimensions . . . . . 4 × 4 mils
Metalization . . . . . Aluminum
Backing . . . . . None
Substrate Potential . . . . . $-V_S$
Passivation . . . . . Oxynitride
Die Attach . . . . . Gold Eutectic
Bond Wire . . . . . 1.25 mil Aluminum; Ultrasonic Bonding or 1 mil Gold; Gold Ball Bonding

APPLICATIONS INFORMATION

Raster scan video displays image data on a line by line basis, with timing and control signals inserted between the lines. The control signals include the horizontal synchronization pulses, which are used to align the display circuitry at the beginning of each line. After the complete video image is displayed on the monitor, the process begins again with the next image. The vertical reset pulse(s) that initiate this timing sequence are located between each video image.



Raster Graphics Configuration for TTL Systems

The image data is distinguished from the timing information by its location relative to the blanking level. The blanking reference level is at the blackest extreme of the image data and all timing signals are designed to fall below the blanking level so as not to be seen on the monitor. The actual image data is located above the blanking level and it may be further separated from the timing signal by the setup level. The setup level is simply a buffer zone between the timing and image data.

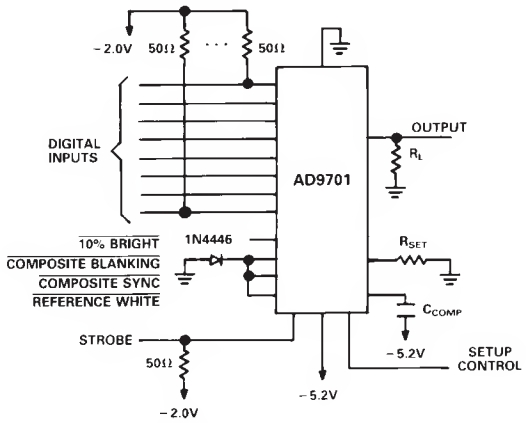
Generation of the timing signals for the AD9701 is controlled by the COMPOSITE BLANKING and the COMPOSITE SYNC inputs. In normal operation, the output level of the AD9701 is forced to the blanking level (black) with the COMPOSITE BLANKING control so that when the synchronization occurs, it will not interfere (be seen) with the monitor image. The COMPOSITE SYNC control forces the output level below the blanking level, generating the synchronization pulse.

The "grey scale" is the image intensity range located above the blanking level by the amount of the setup level. The setup level is "reference black," the darkest displayable picture intensity. The top of the "grey scale" is "reference white" or the brightest picture intensity. As an 8-bit device, the AD9701 divides the "gray scale" into 256 individual levels.

Normal raster scan waveforms divide the region between the blanking level and reference white into 100 IRE units (International Radio Engineers). The setup level can range from 0 to 20 IRE units but typically is around 10 IRE units, and the synchronization pulse level typically falls 40 IRE units below the blanking level. For the AD9701, the reference white level is 10 IRE units below the full-scale output range (0 mA_{OUT}).

In terms of priority, the REFERENCE WHITE control overrides the data inputs, but both COMPOSITE SYNC and COMPOSITE BLANKING override the data inputs and the REFERENCE WHITE control. A fourth control is active at all times, 10% BRIGHT, which adds approximately 10 IRE units to the output level no matter what the input state of the AD9701. The 10% BRIGHT control is primarily used to highlight areas of the video image.

As with any high-speed device, the AD9701 requires a substantial low impedance ground plane and high quality ground connections to achieve the best performance. Performance can also be improved with adequate power supply decoupling near the supply pins of the AD9701. In ECL mode, the output of the AD9701 is designed to drive 75 Ω cable directly, with 75 Ω terminations to ground at both ends of the cable. For TTL configurations, the output should be terminated to +5.0 V through an 82 Ω resistor (see circuit below).

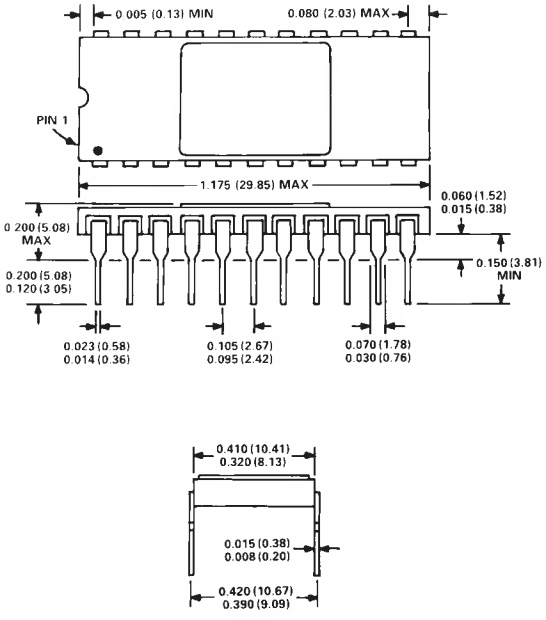


Standard Reconstruction Configuration

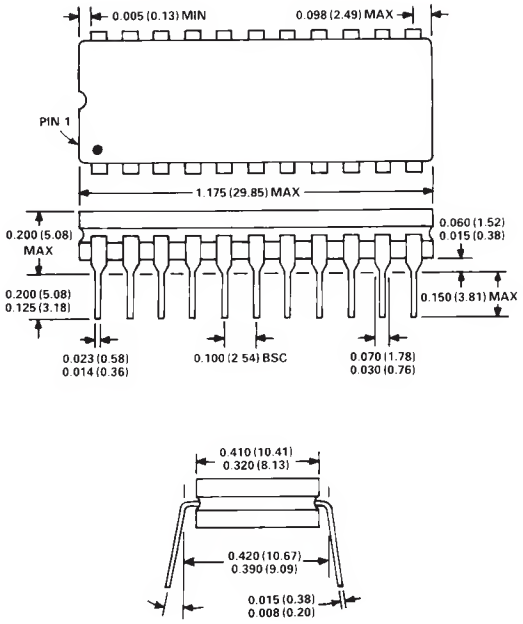
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

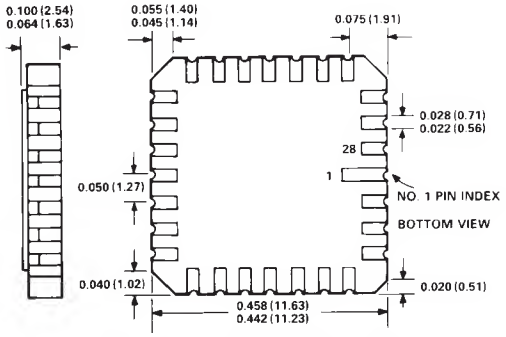
22-Pin Side-Brazed DIP



22-Pin Ceramic DIP



28-Pin LCC



NOTES
1. THIS DIMENSION CONTROLS THE OVERALL PACKAGE THICKNESS.
2. APPLIES TO ALL FOUR SIDES.
3. ALL TERMINALS ARE GOLD PLATED.

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